CLAIMS

1. A shifter circuit capable of shifting a plurality of input data bits to the left or right by a number of bit positions as a function of a binary value of a plurality of shift control bits, comprising:

a first shifter element configured to perform one of two shifting operations on the input data bits to produce a plurality of first output bits, a first one of the shift control bits being used to select the shifting operation performed by the first shifter element;

a second shifter element configured to perform at least one shifting operation on the first output bits to produce a plurality of second output bits, each of said at least one shifting operation being selectable from two shifting operations, a different one of the shift control bits being used to select each of said at least one shifting operation performed by the second shifter element; and

a third shifter element configured to perform one of two shifting operations on the second output bits, a second one of the shift control bits being used to select the shifting operation performed by the third shifter element.

2. The shifter circuit of claim 1 wherein the two shifting operations of the first shifter element comprises a no-shift operation and a right shift operation by one bit position.

3. The shifter circuit of claim 2 wherein the first one of the shift control bits comprises the least significant bit, and wherein the first shifter element is further configured to perform the no-shift operation if the first one of the shift control bits is one and perform the right shift operation if the first one of the shift control bits is zero.

4. The shifter circuit of claim 1 wherein the shift control bits comprise n bits, and wherein the second shifter element comprises $(n-2)$ serial stages, each of the $(n-2)$ stages being configured to perform one of said at least one shifting operation.

5. The shifter circuit of claim 4 wherein an i stage of the $(n-2)$ stages is configured to perform a right or left shift operation by $2^{(i-1)}$ bit positions, where $(1 \leq i \leq (n-2))$.

6. The shifter circuit of claim 5 wherein the i stage of the $(n-2)$ stages is configured to perform the left shift operation if its corresponding shift control bit is one and perform the right shift operation if its corresponding shift control bit is zero.

7. The shifter circuit of claim 1 wherein the shift control bits comprise n bits, and wherein the two shifting operations of the third shifter element comprise a right and left shift operation each by $2^{(n-2)}$ bit positions.

8. The shifter circuit of claim 7 wherein the second one of the shift control bits comprises the most significant bit, and wherein the third shifter element is further configured to perform the left shift operation if the second one of the shift control bits is zero and perform the right shift operation if the second one of the shift control bits is one.

9. The shifter circuit of claim 1 wherein the first and second shifter elements are each configured to retain all the input data bits for any combination of shift operations.

10. The shifter circuit of claim 1 wherein the shift control bits comprise n bits, and wherein the first and third shifter elements each comprises a multiplexer circuit, and the second shifter element comprises a serial arrangement of $(n-2)$ multiplexer circuits.

11. The shifter circuit of claim 10 wherein the input data bits comprise m bits, and wherein each of the multiplexer circuits comprises at least m parallel multiplexers.

12. The shifter circuit of claim 10 wherein the input data bits comprise m bits, and wherein the multiplexer circuit for the first shifter element comprises $(m+1)$ parallel multiplexers.

13. The shifter circuit of claim 12 wherein the i multiplexer circuit of the serial arrangement of $(n-2)$ multiplexer circuits comprises a plurality of parallel multiplexers equal to 2^i multiplexers plus the number of parallel multiplexers from which it receives its inputs, where $(1 \leq i \leq (n-2))$.

14. A shifter circuit capable of shifting a plurality of input data bits to the left or right by a number of bit positions as a function of a binary value of a plurality of shift control bits, comprising:

first shifting means for performing one of two shifting operations on the input data bits to produce a plurality of first output bits, a first one of the shift control bits being used to select the shifting operation performed by the first shifting means;

second shifting means for performing at least one shifting operation on the first output bits to produce a plurality of second output bits, each of said at least one shifting operation being selectable from two shifting operations, a different one of the shift control bits being used to select each of said at least one shifting operation performed by the second shifting means; and

third shifting means for performing one of two shifting operations on the second output bits, a second one of the shift control bits being used to select the shifting operation performed by the third shifting means.

15. The shifter circuit of claim 14 wherein the two shifting operations of the first shifter element comprises a no-shift operation and a right shift operation by one bit position.

16. The shifter circuit of claim 15 wherein the first one of the shift control bits comprises the least significant bit, and wherein the first shifting means is further configured to perform the no-shift operation if the first one of the shift control bits is one and perform the right shift operation if the first one of the shift control bits is zero.

17. The shifter circuit of claim 14 wherein the shift control bits comprise n bits, and wherein the second shifting means comprises $(n-2)$ serial stages, each of the $(n-2)$ stages being configured to perform one of said at least one shifting operation.

18. The shifter circuit of claim 17 wherein an i stage of the $(n-2)$ stages is configured to perform a right or left shift operation by $2^{(i-1)}$ bit positions, where $(1 \leq i \leq (n-2))$.

19. The shifter circuit of claim 18 wherein the an i stage of the $(n-2)$ stages is configured to perform the left shift operation if its corresponding shift control bit is one and perform the right shift operation if its corresponding shift control bit is zero.

20. The shifter circuit of claim 14 wherein the shift control bits comprise n bits, and wherein the two shifting operations of the third shifting means comprise a right and left shift operation each by $2^{(n-2)}$ bit positions.

21. The shifter circuit of claim 20 wherein the second one of the shift control bits comprises the most significant bit, and wherein the third shifter element is further configured to perform the left shift operation if the second one of the shift control bits is zero and perform the right shift operation if the second one of the shift control bits is one.

22. A method of shifting a plurality of input data bits to the left or right by a number of bit positions as a function of a binary value of a plurality of shift control bits, comprising:

performing a shifting operation on the input data bits to produce a plurality of first output bits, and using a first one of the shift control bits to select, from two shifting operations, the shifting operation performed on the input data bits;

performing at least one shifting operation on the first output bits to produce a plurality of second output bits, and using a different one of the shift control bits to select, from two shifting operations, each of said at least one shifting operation performed on the first output bits; and

performing a shifting operation on the second output bits, and using a second one of the shift control bits to select, from two shifting operations, the shifting operation performed on the second output bits.

23. The method of claim 22 wherein the two shifting operations from which the shifting operation performed on the input data bits is selected comprises a no-shift operation and a right shift operation by one bit position.

24. The method of claim 23 wherein the first one of the shift control bits comprises the least significant bit, and wherein the shifting operation performed on the input data bits is the no-shift operation if first one of the shift control bits is one.

25. The method of claim 23 wherein the first one of the shift control bits comprises the least significant bit, and wherein the shifting operation performed on the input data bits is the right shift operation if the first one of the shift control bits is zero.

26. The method of claim 22 wherein the shift control bits comprise n bits, and wherein the at least one shifting operation performed on the first output bits is performed by $(n\text{-}2)$ serial stages, each of the $(n\text{-}2)$ stages performing one of said at least one shifting operation.

27. The method of claim 26 wherein an i stage of the $(n\text{-}2)$ stages perform a right or left shift operation by $2^{(i-1)}$ bit positions, where $(1 \leq i \leq (n\text{-}2))$.

28. The method of claim 27 wherein the an i stage of the $(n\text{-}2)$ stages performs the left shift operation if its corresponding shift control bit is one.

29. The method of claim 27 wherein the an i stage of the $(n\text{-}2)$ stages performs the right shift operation if its corresponding shift control bit is zero.

30. The method of claim 22 wherein the shift control bits comprise n bits, and wherein the two shifting operations from which the shifting operation performed on the second output bits is selected comprises a right and left shift operation each by $2^{(n-2)}$ bit positions.

31. The method of claim 30 wherein the second one of the shift control bits comprises the most significant bit, and wherein the shifting operation performed on the second output bits is the left shift operation if the second one of the shift control bits is zero.

32. The method of claim 30 wherein the second one of the shift control bits comprises the most significant bit, and wherein the shifting operation performed on the second output bits is the right shift operation if the second one of the shift control bits is one.